LIST OF REFERENCES CITED BY APPLICANT *(Use several sheets if necessary)*	ATTY. DOCKET NO. 100665.0044US1	SERIAL NO. 10/026,338
	APPLICANT Jesse Pedigo	
	FILING DATE 12/20/01	GROUP 1725

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
KS		3,601,523	08/24/71	Through Hole Connectors	174	68.5	06/19/70
		4,106,187	08/15/78	Curved Rigid Printed Circuit Boards	29	625	01/16/76
		4,283,243	08/11/81	Use of Photosensitive Stratum to Create Through-Hole Connections in Circuit Boards	156	237	03/20/80
		4,360,570	11/23/82	Use of Photosensitive Stratum to Create Through-Hole Connections in Circuit Boards	428	596	06/15/81
		4,622,239	11/11/86	Method and Apparatus for Dispensing Viscous Materials	427	96	02/18/86
		4,700,474	10/20/87	Apparatus and Method for Temporarily Sealing Holes in Printed Circuit Boards	29	846	11/26/86
		4,777,721	10/18/88	Apparatus and Method for Temporarily Sealing Holes in Printed Circuit Boards Utilizing a Thermodeformable Material	29	846	10/15/87
		4,783,247	11/8/88	Method and Manufacture for Electrically Insulating Base Material Used in Plated-Through Printed Circuit Panels	204	181.1	05/15/86
		4,884,337	12/05/89	Method for Temporarily Sealing Holes in Printed Circuit Boards Utilizing a Thermodeformable Material	29	846	10/15/87
		4,964,948	10/23/90	Printed Circuit Board Through Hole Technique	156	659	11/13/89
		4,995,941	02/26/91	Method of Manufacture Interconnect Device	156	630	05/15/89
		5,053,921	10/01/91	Multilayer Interconnect Device and Method of Manufacture Thereof	361	386	10/23/90
		5,058,265	10/22/91	Method for Packaging a Board of Electronic Components	29	852	09/10/90
		5,145,691	09/08/92	Apparatus for Packing Filler into Through-Holes or the Like in a Printed Circuit Board	425	110	03/22/91
		5,220,723	06/22/93	Process for Preparing Multi-Layer Printed Wiring Board	29	830	11/04/91
		5,274,916	01/04/94	Method of Manufacturing Ceramic Multilayer Electronic Component	29	848	12/17/92
		5,451,721	09/19/95	Multilayer Printed Circuit Board and Method for Fabricating Same	174	261	09/24/91
KS		5,456,004	10/10/95	Anisotropic Interconnect Methodology for Cost Effective Manufacture of High Density Printed Circuit Boards	29	852	01/04/94

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KS		5,471,09[illegible]	[illegible]1/28/95	Techniques for Via Formation and Filling	257	752	08/26/91
		5,532,[illegible]26	07/02/96	Techniques for Via Formation and Filling	257	752	03/28/95
		5,540,77[illegible]	[illegible]7/30/96	Apparatus for Manufacture of Multi-Layer Ceramic Interconnect Structures	118	692	03/01/95
		5,578,151	11/26/96	Manufacture of A Multi-Layer Interconnect Structure	156	64	03/01/95
		5,591,353	01/07/97	Reduction of Surface Copper Thickness on Surface Mount Printed Wire Boards with Copper Plated Through Holes by the Chemical Planarization Method	216	18	08/18/94
		5,610,103	03/11/97	Ultrasonic Wave Assisted Contact Hole Filling	437	225	12/12/95
		5,637,834	06/10/97	Multilayer Circuit Substrate and Method for Forming Same	174	264	02/03/95
		5,662,987	09/02/97	Multilayer Printed Wiring Board and Method of Making Same	428	209	02/01/96
		5,699,613	12/23/97	Fine Dimension Stacked Vias for a Multiple Layer Circuit Board Structure	29	852	09/25/95
		5,744,285	04/28/98	Composition and Process for Filling Vias	430	318	07/18/96
		5,753,976	05/19/98	Multi-Layer Circuit Having a Via Matrix Interlayer Connection	257	774	06/14/96
		5,761,803	06/09/98	Method of Forming Plugs in Vias of A Circuit Board by Utilizing a Porous Membrane	29	852	06/26/96
		5,766,670,	06/16/98	Via Fill Compositions for Direct Attach of Devices and Methods for Applying Same	427	8	11/17/93
		5,822,856	10/20/98	Manufacturing Circuit Boards Assemblies Having Filled Vias	29	832	06/28/96
KS		5,824,155	10/20/98	Method and Apparatus for Dispensing Viscous Material	118	410	11/08/95

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER REFERENCES (*Including Author, Title, Date, Pertinent Pages, Etc.*)

EXAMINER	DATE CONSIDERED
Kelly Hou	7-8-03

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with **MPEP 609**; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

LIST OF REFERENCES CITED BY APPLICANT *(Use several sheets if necessary)*	ATTY. DOCKET NO. 100970.665044US1	SERIAL NO. 10/026338
	APPLICANT Pedigo, Jesse et al	
	FILING DATE 20 December 2001	GROUP To be determined

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
KS	AA	6,193,144	02/27/01	Paste Providing Method, Soldering Method and Apparatus and System Therefor	228	248	06/22/98
KS	BB	6,491,204	12/10/02	Stencil Wiping Device	228	22	11/22/00
	CC						
	DD						
	EE						
	FF						
	GG						
	HH						
	II						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	JJ							
	KK							
	LL							
	MM							
	NN							

OTHER REFERENCES (*Including Author, Title, Date, Pertinent Pages, Etc.*)

KS	OO	Shoji Oikawa et al., Solder Coating Device, May 27, 1987, pages unknown

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	7-8-03

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